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A Novel Multilevel Inverter Topology with Reduced Switches using Fuzzy Controller

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Abstract: Multilevel inverter has become popular in recent years for high power applications. Their major drawbacks are complexity, required more numbers of power devices and complex control circuitry. This paper proposes fuzzy logic controller based a new multilevel inverter topology using an H bridge output stage with three bidirectional auxiliary switch. In the proposed circuit configuration the inverter produces nine levels including a zero. The new topology produces a significant reduction in the number of power devices and capacitors required to implement a multilevel output when compared to the conventional MLIs. The Total Harmonic Distortions generated by multilevel inverter can greatly reduced by fuzzy logic control scheme. In this proposed work the harmonics distortion was reduced by using Fuzzy Logic Control scheme, which increases the performance of the multilevel inverter.

Keywords: H-Bridge, Multilevel inverter, Fuzzy logic, Bidirectional Switch, Total Harmonic Distortion (THD)

I INTRODUCTION

The multilevel inverter was first introduced in 1975. The first multilevel inverter introduced was three level inverter. A multilevel inverter is a power electronic system that forms a desired output voltage from single dc voltage as input. With an increasing number of auxiliary switches, the inverter output voltage waveform approaches a nearly sinusoidal waveform while using a fundamental frequency switching scheme. The various topologies presented in the literature as multilevel inverters [1] shows a number of characteristics in common. The advantages of multilevel inverters are

-reduction in the voltages applied to the main power switches, enabling operation at higher load voltages.
-reduction in the commutation frequency applied to the power components
-transient voltages automatically limited.

The major drawbacks associated with the multilevel configurations are their circuit complexity it requires more number of power switches that must be commutated in a exactly determined sequence by a dedicated modulator circuit.

In the past, these disadvantages were almost overwhelming; due to the cost differences they produced between multilevel and standard configurations. Multilevel converters were used only in some high power applications such as high power motor drivers in marine, mining, or chemical industries applications, high power transmission, power line conditioners, etc. [2]–[11]. In all these applications their advantages compensate the cost differential. Multilevel inverters are promising; they have nearly sinusoidal output-voltage waveforms, output current with better harmonic profile, less stressing of electronic components owing to decreased voltages, switching losses that are lower than those of conventional two-level inverters, a smaller filter size, and lower EMI, all of which make them cheaper, lighter, and more compact [12], [13].

Various topologies for multilevel inverters have been proposed over the years. Common ones are diode-clamped [14]–[19], flying capacitor or multicell [20]–[26], cascaded H-bridge [17]–[30], and modified H-bridge multilevel [1].

A single-phase inverter is usually used for residential or low-power applications of power ranges that are less than a kW. One of the significant advantages of multilevel inverters configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output.

The output voltage waveform of a multilevel inverter is composed of the number of voltages, typically obtained from capacitor voltage sources. Multilevel starts from three levels. As number of levels reach infinity, the output THD approaches zero. The number of the achievable voltage levels, however, is limited by voltage unbalance problems, voltage clamping requirement, circuit layout and packaging constraints.

A generalized circuit configuration of the new topology is shown in Fig.1 the proposed inverter topology is developed from this general configuration which has the advantages of the reduced number of power switching devices. The percentage reduction in the number of power switches compared to conventional H-bridge multilevel inverter is shown in Table 1.

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TABLE I Comparison between Two Inverter Topology and Four Different Levels

Inverter type	Number of switches			
	5- level	7- level	9- level	11- level
Cascaded	8	12	16	20
Proposed Topology	5	6	7	8
% Reduction	37.5%	50%	56.25%	60%

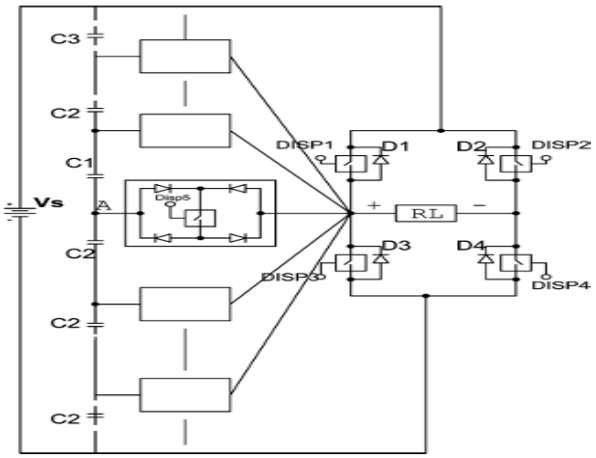

Fig. 1 Generalized Multilevel Inverter Configuration of the New Topology

This new topology has the advantage of its reduced number of switching devices compared to the conventional cascaded H-bridge and diode-clamped multilevel inverters for the same number of levels. It can also be extended to any number of levels.

The modes of operation of a 9-level inverter are presented, where similar modes can be realized for higher levels. The inverter operation is controlled using switching angles based on PWM with help of pulse generator. These angles are obtained from solving the waveform equations using the theory of resultants.

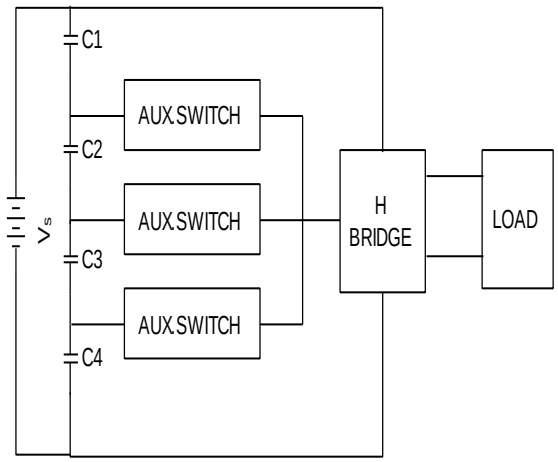

Fig. 2 New Topology Block Diagram of Nine Level Inverter

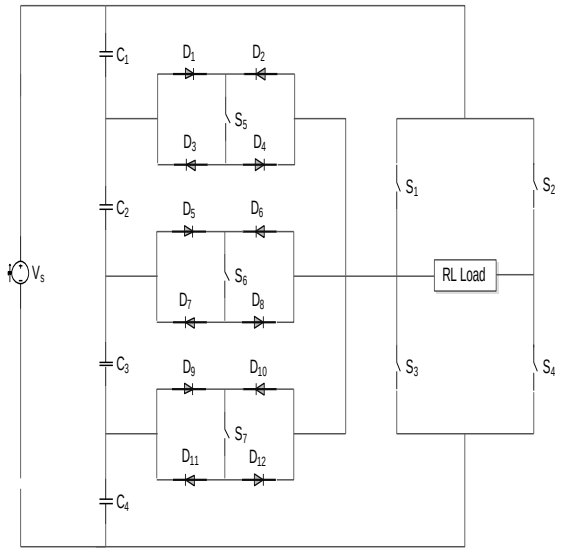

Fig. 3 Proposed Nine Level H Bridge Inverter Topology

Simulation of higher levels of the proposed inverter topology is carried out using MATLAB the validity of the proposed topology and the harmonic elimination method are verified experimentally for 9 level inverters. This paper presents how reduced harmonic distortion is achieved for a new topology of multilevel inverters using programmed PWM technique.

II. MULTILEVEL INVERTER TOPOLOGY

The single-phase nine-level inverter was developed from the generalized inverter as shown in Fig.1. It comprises a single-phase conventional H-bridge inverter, three bidirectional switches, and a capacitor voltage divider formed by C1, C2,C3 and C4, , as shown in Fig. 3. The modified H-bridge topology is significantly advantageous over other topologies, i.e., less power switch, power diodes, and less capacitor for inverters of the same number of levels.

Proper switching of the inverter can produce nine-output-voltage-levels (V_{dc}, 3 V d c /4, V d c /2, V d c /4, 0 , $-V_{dc}/4$, $-V_{dc}/2$, $-3V_{dc}/4$, $-V_{dc}$) from the dc supply voltage. The proposed inverter's operation can be divided into nine switching states. The required nine levels of output voltage were generated as follows.

Maximum positive output (V_{dc}): S_1 is ON connecting the load positive terminal to V_{dc} and S_4 is ON connecting the load negative terminal to ground. All other controlled switches are OFF. The voltage applied to the load terminals is $V_{dc.}$ Fig.2(a) shows the current paths that are active at this stage.

Three-fourth positive output ($3V_{dc}/4$): The bidirectional switch S_5 is ON, connecting the load positive terminal, and S_4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF. The voltage applied to the load terminals is $3V_{dc}/4$

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Half of the positive output ($V_{dc}/2$): the bidirectional switch S_6 is ON, connecting the load positive terminal and S_4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF. The voltage applied to the load terminals is $V_{dc}/2$.

One-fourth of the positive output ($V_{dc}/4$): The bidirectional switch S_7 is ON, connecting the load positive terminal, and S_4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF. The voltage applied to the load terminals is $V_{dc}/4$.

Zero output: This level can be produced by two switching combinations switches S_3 and S_4 are ON, or S_1 and S_2 are ON, and all other controlled switches are OFF. Terminal ab is short circuit, and the voltage applied to the load terminals is zero.

One-fourth negative output ($-V_{dc}/4$): The bidirectional switch S_5 is ON, connecting the load positive terminal, and S_2 is ON, connecting load negative to V_{dc}. All other controlled switches are OFF. The voltage applied to the load terminal is $-V_{dc}/4$.

Half of the negative output ($-V_{dc}/2$): The bidirectional switch S_6 is ON, connecting the load positive terminal and S_2 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF. The voltage applied to the load terminals is $-V_{dc}/2$

Three-fourth negative output ($-3V_{dc}/4$): The bidirectional switch S_7 is ON, connecting the load positive terminal, and S_2 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF. The voltage applied to the load terminals is $-3V_{dc}/4$.

Maximum negative output ($-V_{dc}$): S_2 is ON, connecting the load negative terminal to V_{dc} and S_3 is ON, connecting the load positive terminal to ground. All other controlled switches are OFF. The voltage applied to the load terminals $-V_{dc}$.

Table II shows the switching combinations that generate the required nine output levels (V_{dc}, $3Vdc/4$, $Vdc/2$, $Vdc/4$, 0, $-V_{dc}/4$, $-V_{dc}/2$, $-3V_{dc}/4$,- V_{dc}). In this configuration the four capacitor in the capacitive voltage divider are directly connected across the DC bus and since all switching combinations are activated in an output cycle, the dynamic voltage balance between the two capacitors is automatically restored.

TABLE II Switching Combinations Required To Generate The Nine Level Output Voltage Waveform

S_1	S_2	S_3	S_4	S_5	S_6	S_7	V_{out}
On	Off	Off	On	Off	Off	Off	V_{dc}
Off	Off	Off	On	On	Off	Off	$3V_{dc}/4$
Off	Off	Off	On	Off	On	Off	$V_{dc}/2$
Off	Off	Off	On	Off	Off	On	$V_{dc}/4$
On	On	Off	Off	Off	Off	Off	0
Off	On	Off	Off	On	Off	Off	$-V_{dc}/4$
Off	On	Off	Off	Off	On	Off	$-V_{dc}/2$
Off	On	Off	Off	Off	Off	On	$-3V_{dc}/4$
Off	On	On	Off	Off	Off	Off	$-V_{dc}$

III.FUZZYLOGIC CONTROL

Fuzzy logic control is the evaluation of a set of simple linguistic rules to determine the control action. To develop the rules of the fuzzy logic is needed the good understanding of the process to be controlled, but it does not require a complicated mathematical model. Due to the lack of conventional controller is used for more robust and fast result.

In a fuzzy logic control system, is no necessity for a plant model. The plant can be single input single output or multi-input multi-output. The configuration of fuzzy logic control scheme is shown in Fig.4. Fuzzy logic controller is composed of three parts such as fuzzification; inference engine and defuzzification are described below.

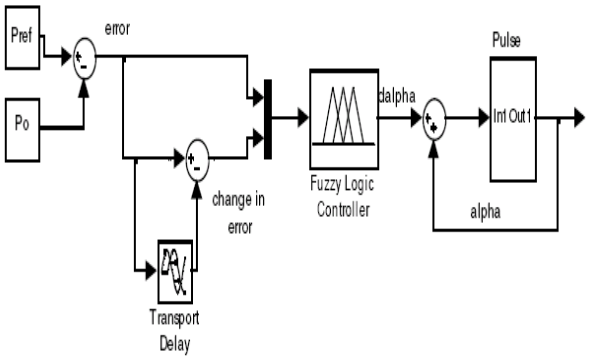

Fig 4: Configuration of Fuzzy Logic Controller

FUZZIFICATION

To translate the values of error and change in error in to fuzzy variable error is assigned with seven fuzzy variables called negative big (nb), negative medium (nm), negative small (ns), zero (zr), positive small (ps),positive medium (pm) and positive big (pb).

Similarly change in error and change alpha also assigned with that seven fuzzy variables. Error(e) and change in error(de) are the input variables, where e is difference between the reference power (Pref) and the actual power (Pout) of system.

Change in error(de) calculated by using sampling interval. The output from the fuzzy logic controller is the change in firing angle (dalpha). Triangular membership functions (trimf) are selected d for all these variables. The membership functions of the each variables error, change in error and change in firing angle are shown in Fig.4.1, Fig.4.2 and Fig.4.3 respectively.

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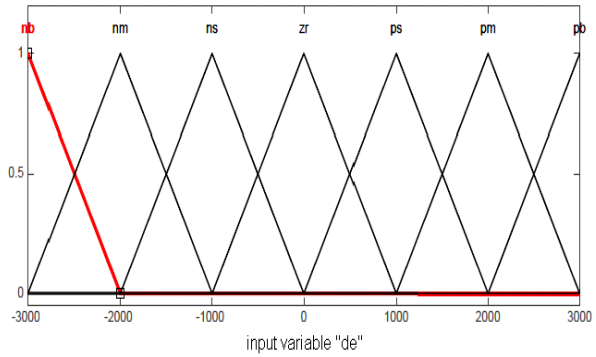

Fig. 4.1: Membership Function for Error (e)

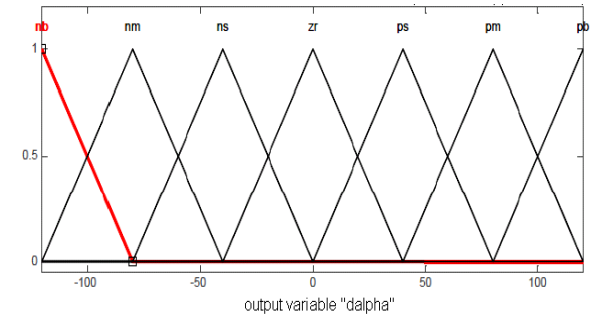

Fig. 4.2: Membership Function for Change in Error (de)

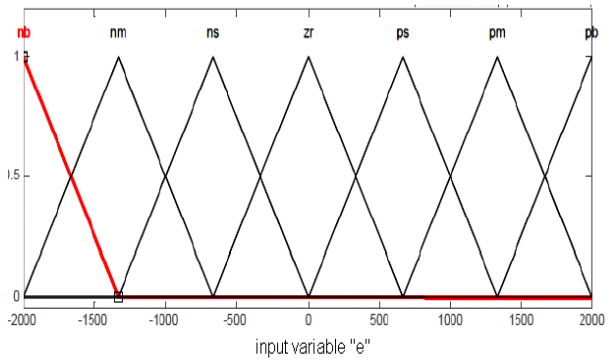

Fig. 4.3: Membership Function for Firing Angle(dalpha)

INTERFRENCE ENGINE

Inference engine performs three tasks: applying fuzzy operator, applying implication method and aggregating all outputs. Inference engine mainly consists of two sub blocks namely, fuzzy rule base and fuzzy implication.

The inputs which are now fuzzified are fed to the inference engine and the rule base is then applied. The output fuzzy sets are then identified using fuzzy implication method.

Table 3shows the rule base of fuzzy logic controller, where all the entries of the matrix are fuzzy sets of error(e), change in error(de) and change in firing angle(dalpha) to the inverter by using fuzzy implication method is min-max.

The consequent fuzzy region is restricted the minimum (min) of the predicate truth while selecting output fuzzy set. The output fuzzy region is updated by taking maximum (max) of these minimized fuzzy sets during shaping of output fuzzy space.

TABLE III Fuzzy Membership Function for Proposed FLC

	Rate of change of error (Δe)						
Error (e)	n	n	nb	nb	nm	n	z
	n	n	nb	nm	n	z	p
	n	n	nm	n	z	p	pm
	n	nm	n	z	p	pm	P
	nm	n	z	p	pm	p	P
	n	z	p	pm	p	p	P
	z	p	pm	pb	p	p	p

DEFUZZIFICATION

The input for the defuzzification process is a fuzzy set and the output is a single number. For the final desired output a non-fuzzy value of control, a defuzzification stage is required. In the proposed scheme bisector defuzzification method is used for defuzzification.

IV MATLAB SIMULINK MODEL AND SIMULATION RESULT

MATLAB SIMULINK model was simulated for proposed configuration before it was physically implemented in a prototype. A nine level inverter model is constructed in MATLAB Simulink software. The new Fuzzy logic controller strategy with reduced number of switches is employed

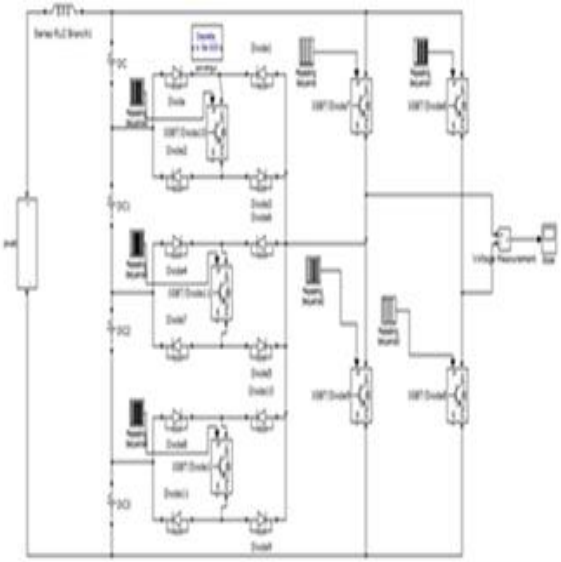

Fig.5 MATLAB/SIMULINK Model of Proposed Nine Level Inverter

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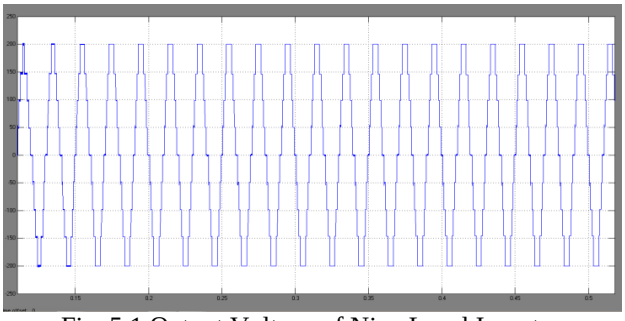

Fig. 5.1 Output Voltage of Nine Level Inverter

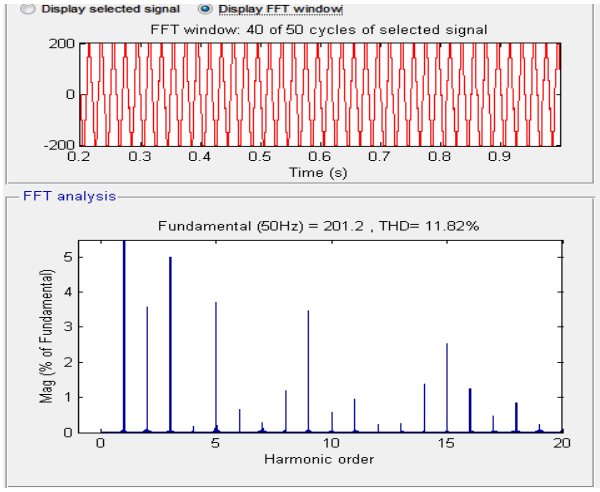

Fig. 6 Harmonic Analysis of Simulated Output

V. CONCLUSION

Multilevel inverters offers improved output waveforms and lower THD. The experimental circuit and simulated result show that clearly the new multilevel topology with three bidirectional auxiliary switches works as expected to generate the required nine level output using only seven power switches and four capacitors. This configuration reduced circuit complexity will be adequate for low-medium power applications where standard multilevel inverter cannot compete with two-level configurations due to cost, such as low-medium power UPS systems. The behavior of the proposed multilevel inverter was analyzed in detail and the desired number of levels of the inverter's output voltage can be achieved. The THD is less in the nine-level inverter compared with that in the seven, five and three-level inverters A further development of the proposed topology can able to be applied to any number of voltage levels within the power switches maximum voltage. As shown in generalized multilevel inverter configuration.

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